

FIG. 3-2

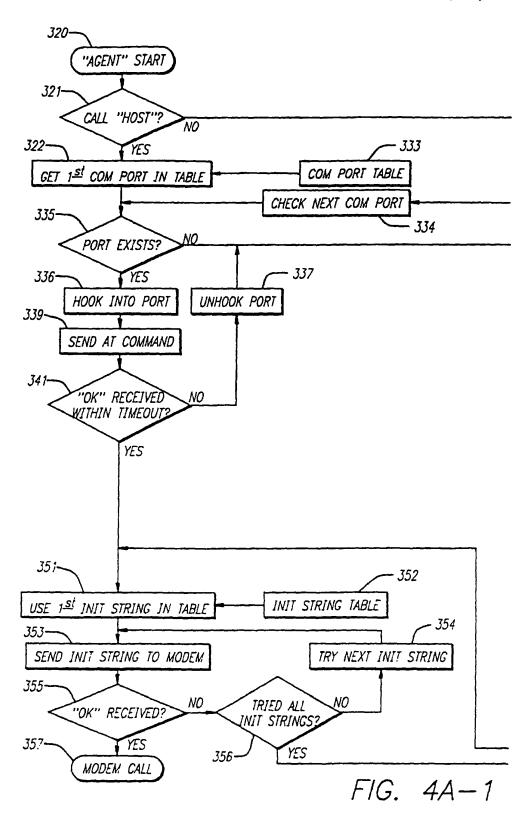
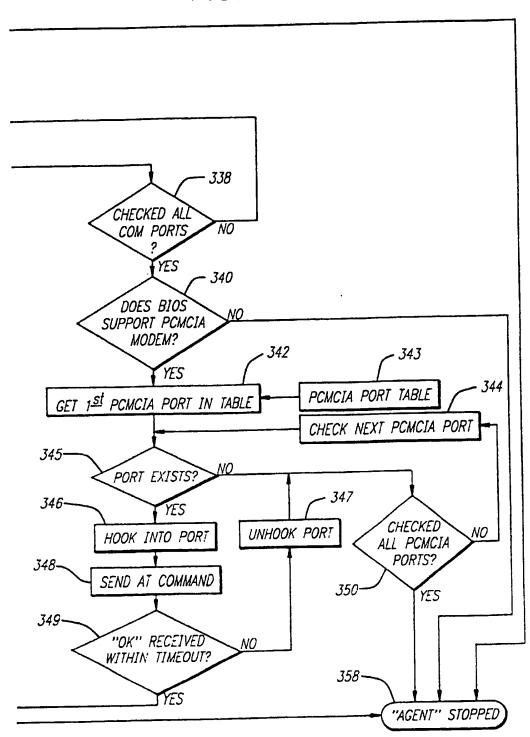


FIG. 4A-2



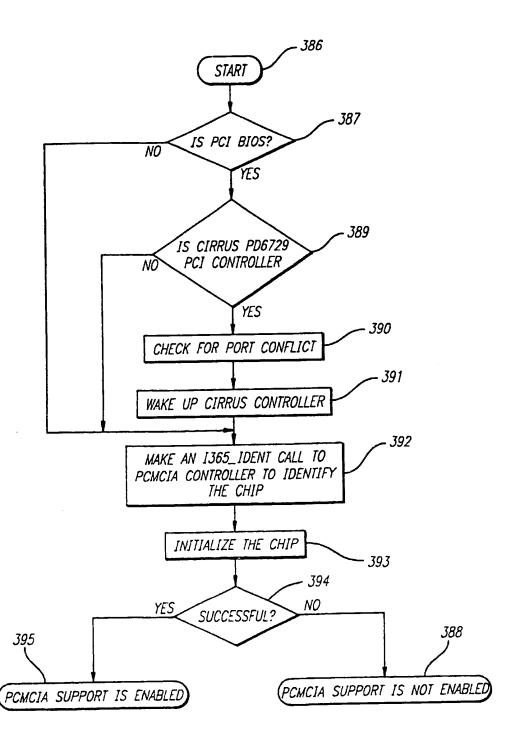
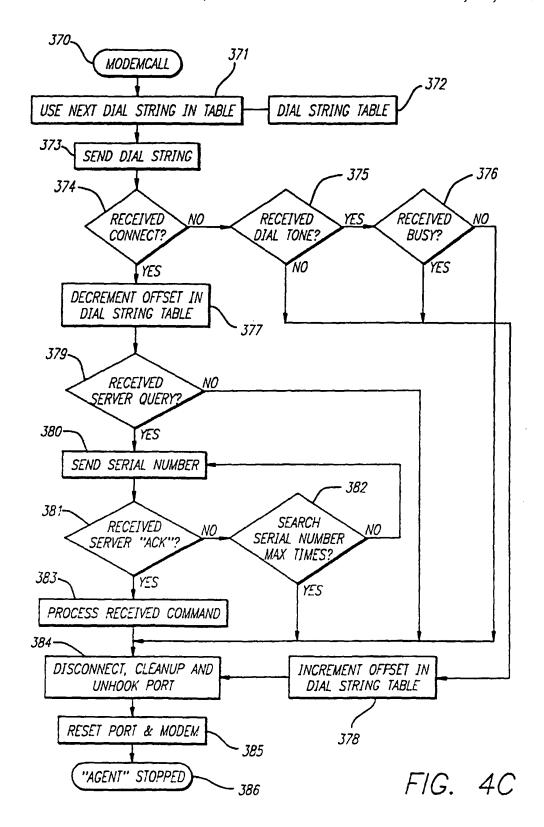
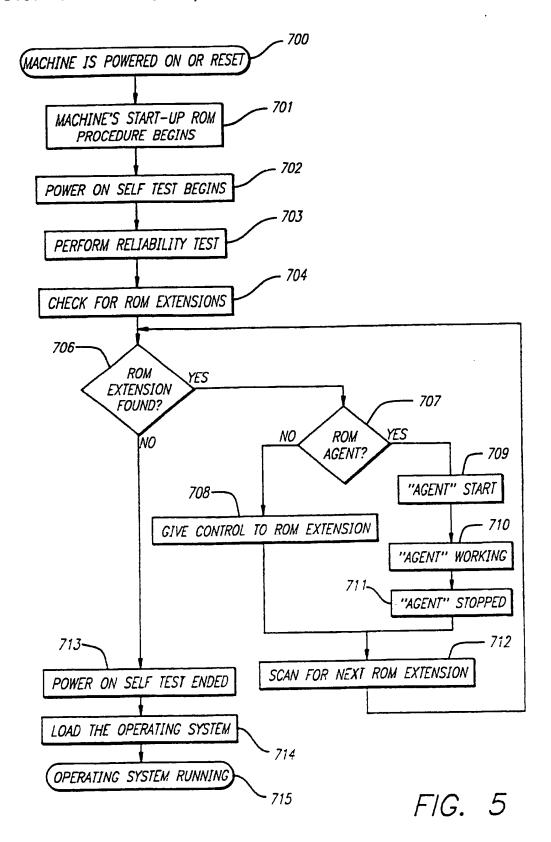
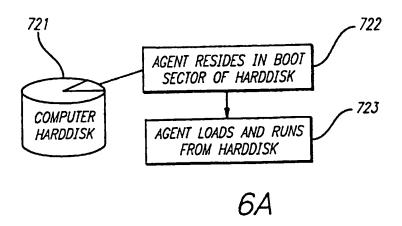


FIG. 4B







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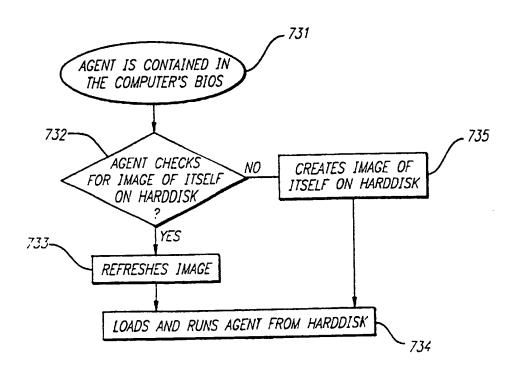


FIG. 6C

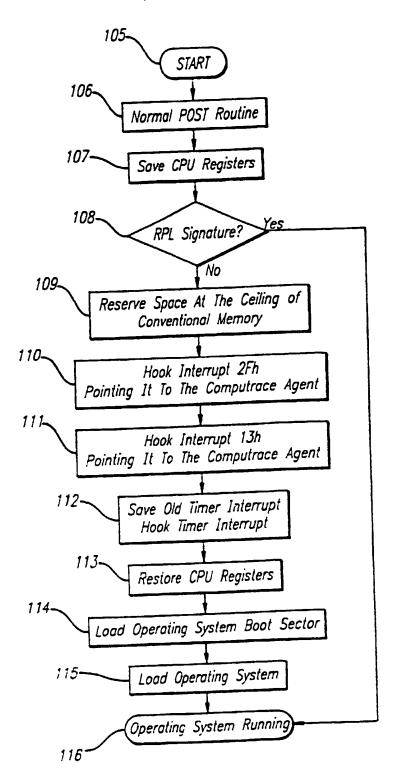


FIG. 6B

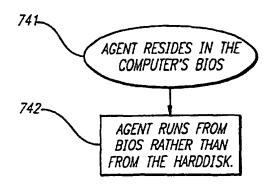


FIG. 6D

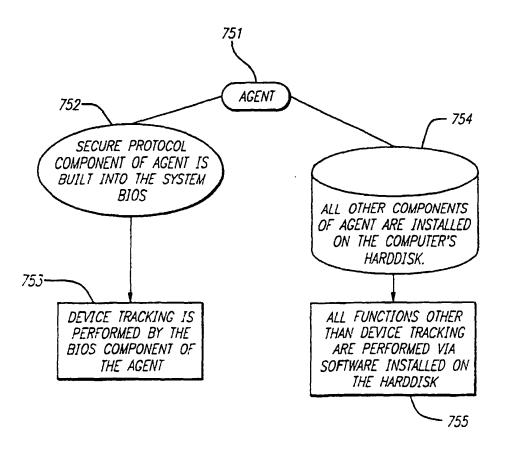
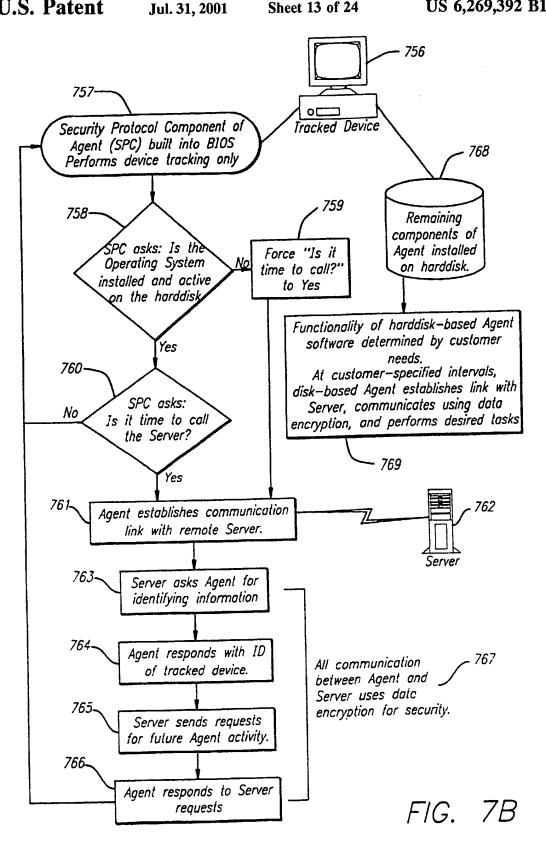


FIG. 7A



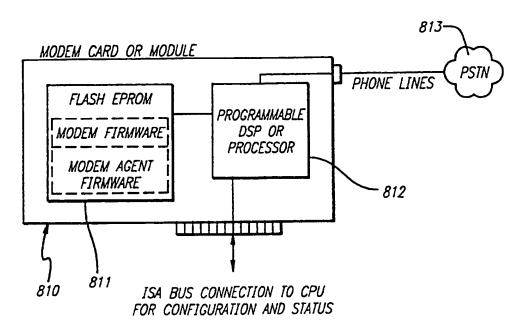
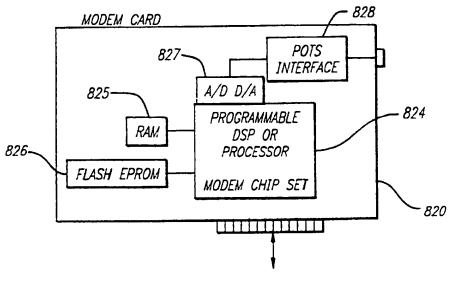


FIG. 8A



ISA BUS CONNECTION TO CPU MAPPED TO I/O PORT ADDRESS

FIG. 8B

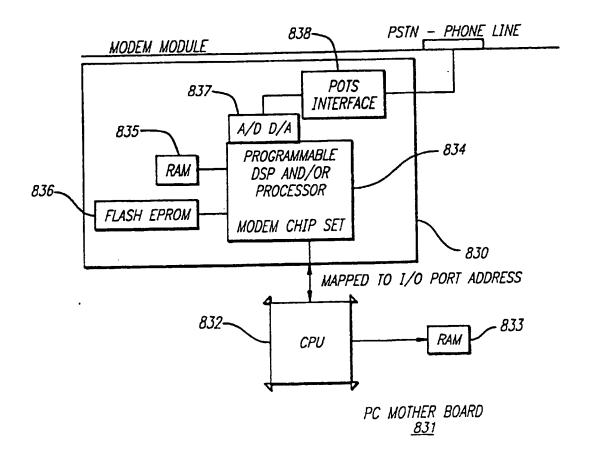


FIG. 8C

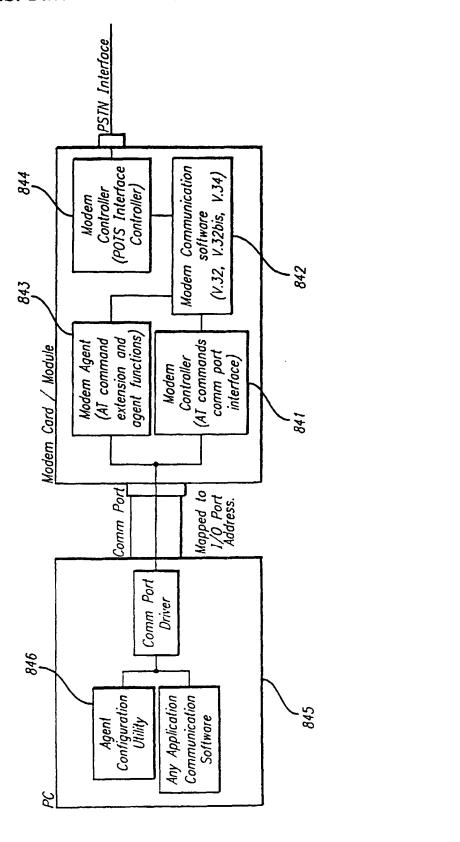
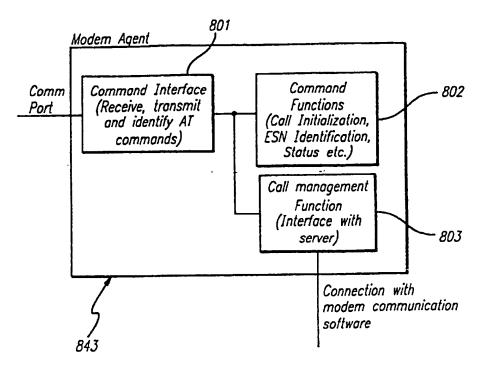
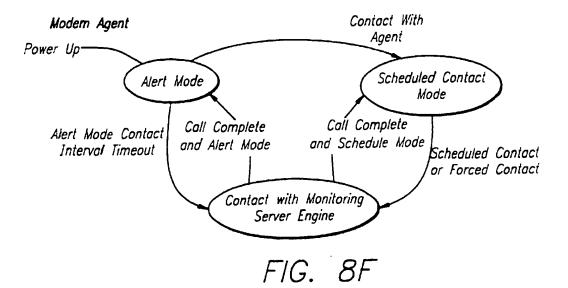


FIG. 8D



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FIG. 8E



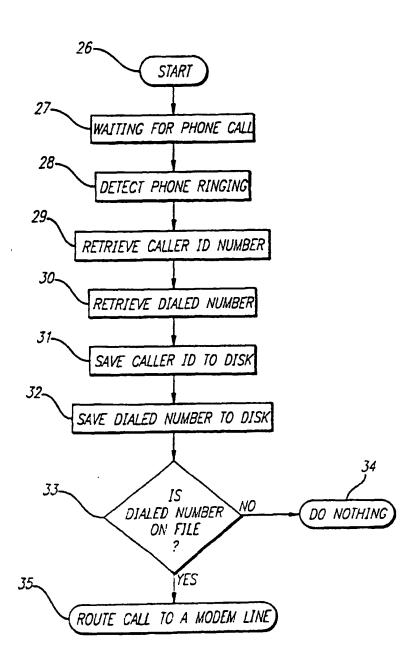
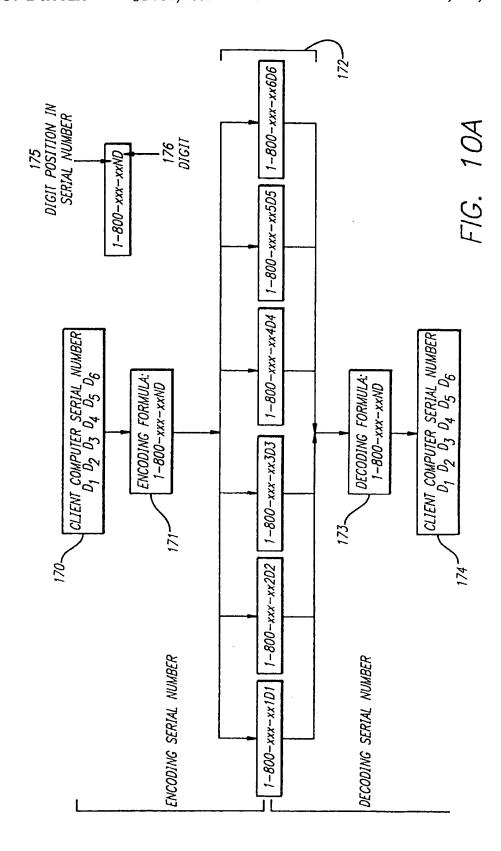
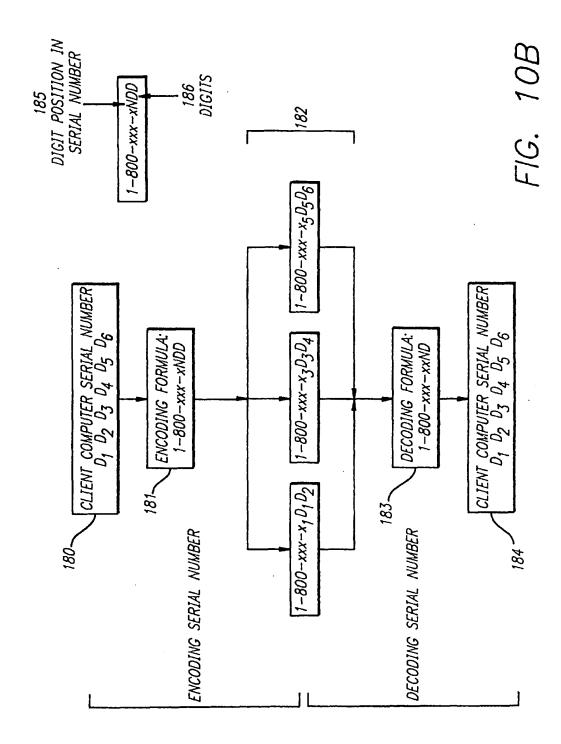
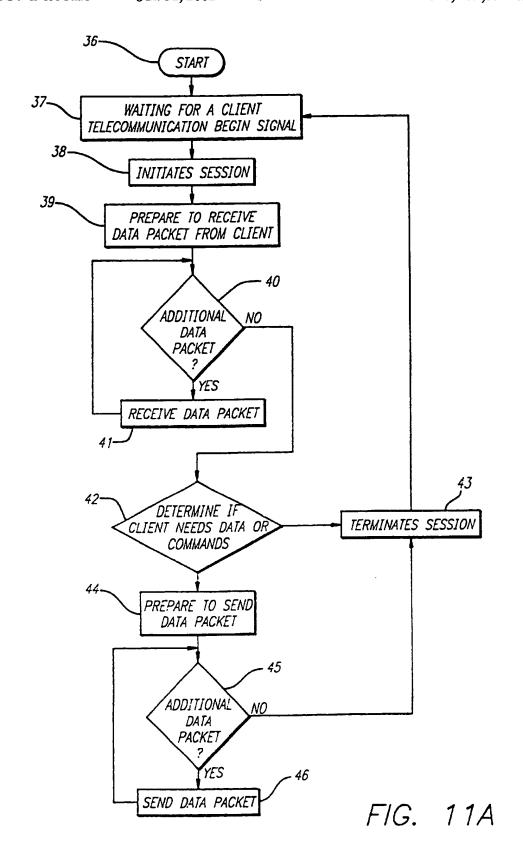


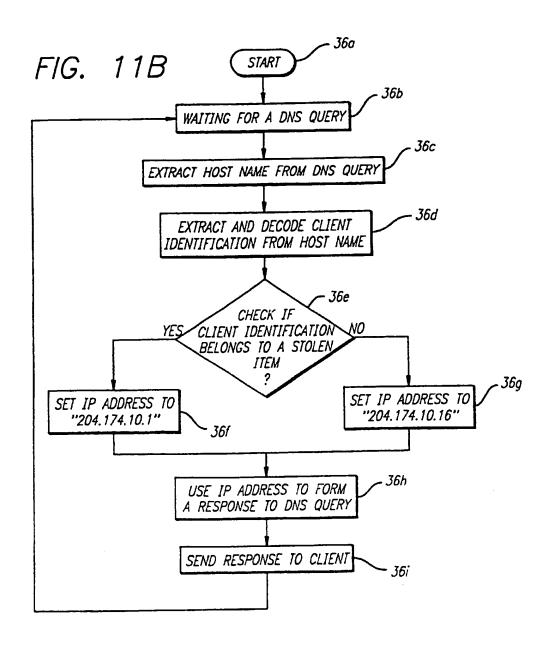
FIG. 9

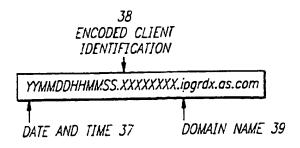






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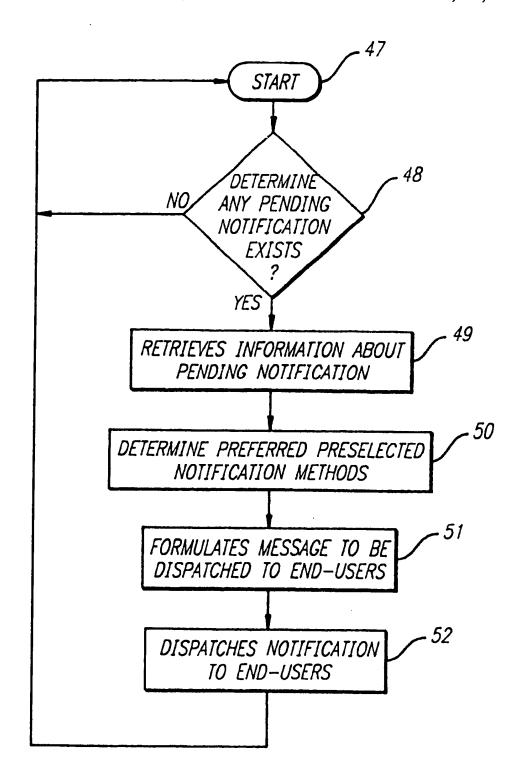
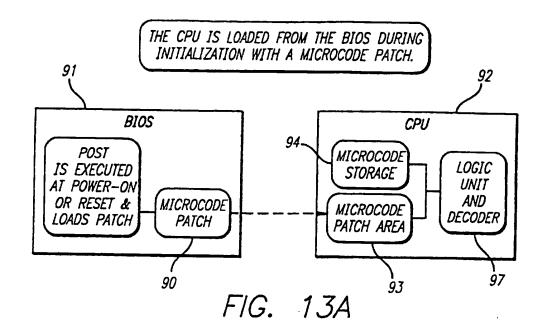


FIG. 12



THE SECURITY PROTOCOL COMPONENT IN THE MICROCODE PATCH INITIATES COMMUNICATION WITH THE MODEM ASYNCHRONOUSLY OF THE NORMAL CODE STREAM (i.e. THE OPERATING SYSTEM OR APPLICATION).

